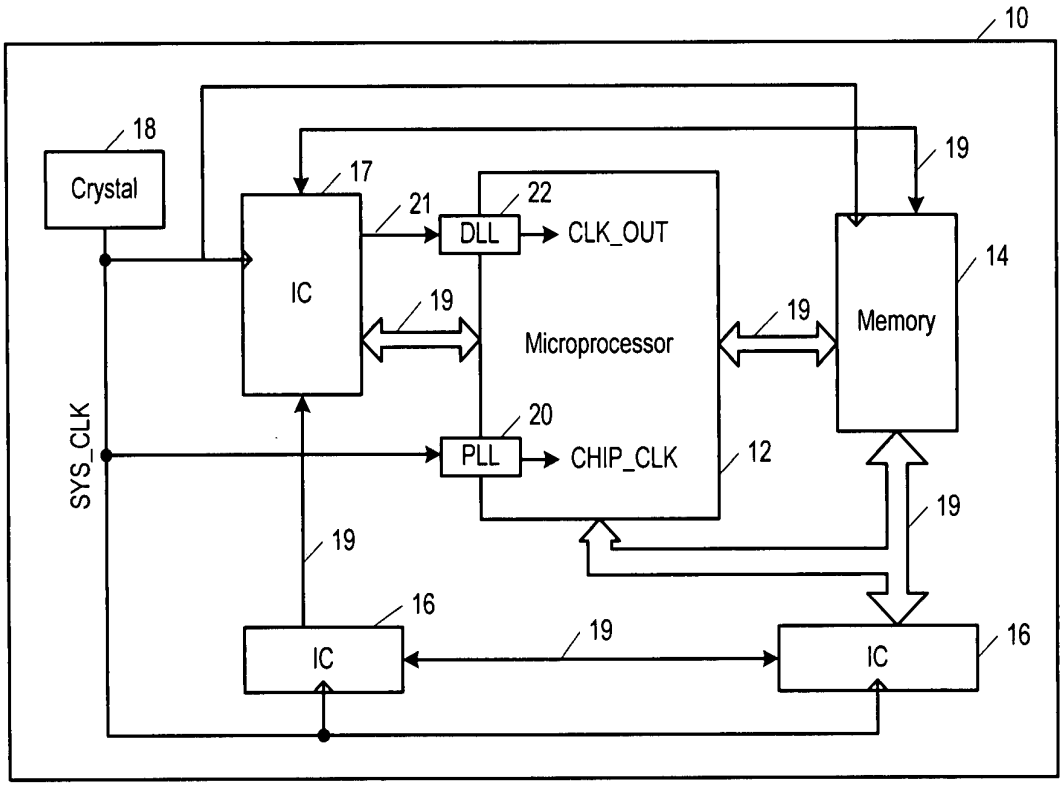

Figure 1
(Prior Art)

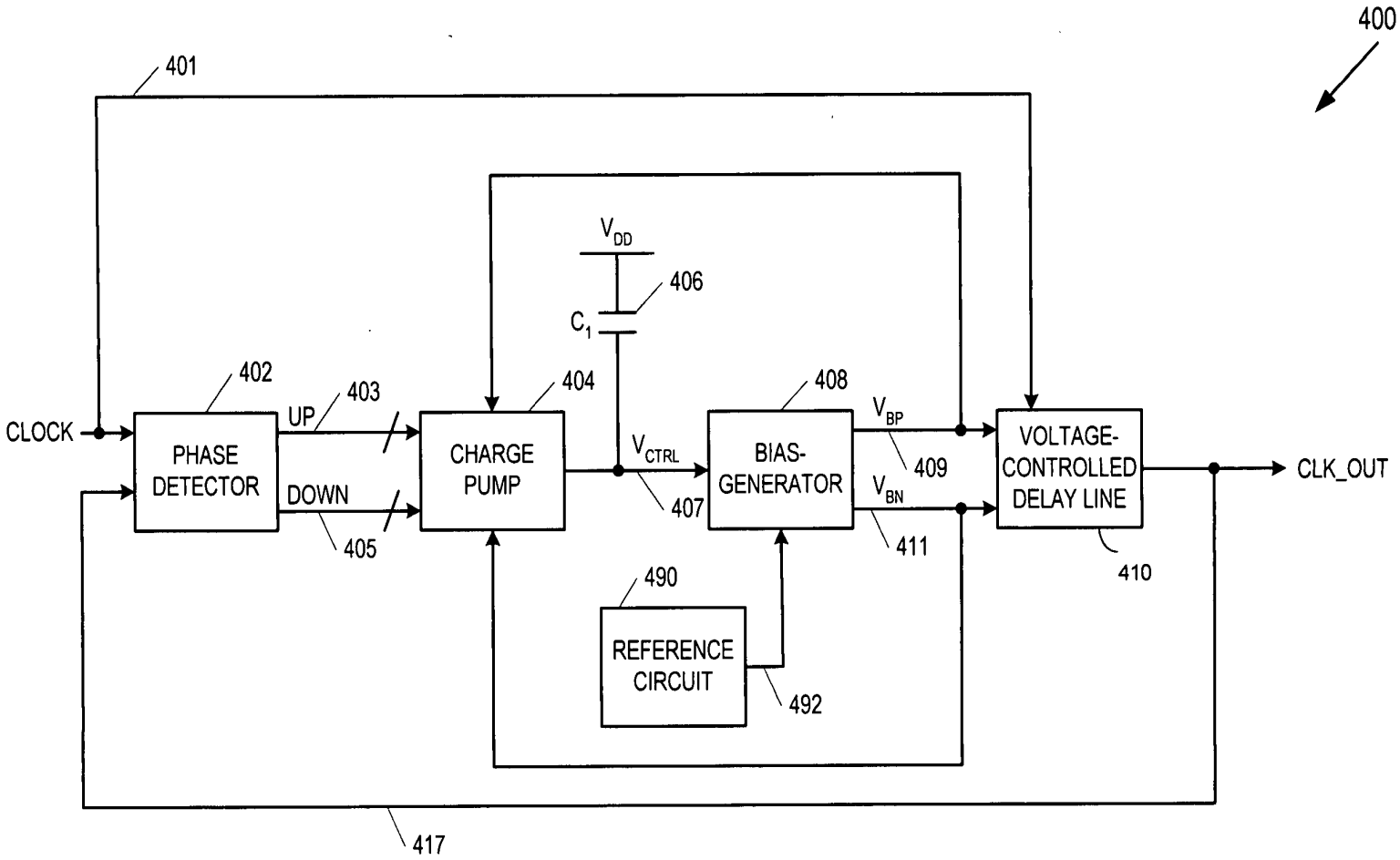
400
401
V_{DD}
406
C_1
402
403
404
408
V_{BP}
CLOCK
PHASE DETECTOR
UP
DOWN
CHARGE PUMP
V_{CTRL}
BIAS-GENERATOR
409
V_{BN}
VOLTAGE-CONTROLLED DELAY LINE
CLK_OUT
405
407
411
410
490
REFERENCE CIRCUIT
492
417

Figure 2

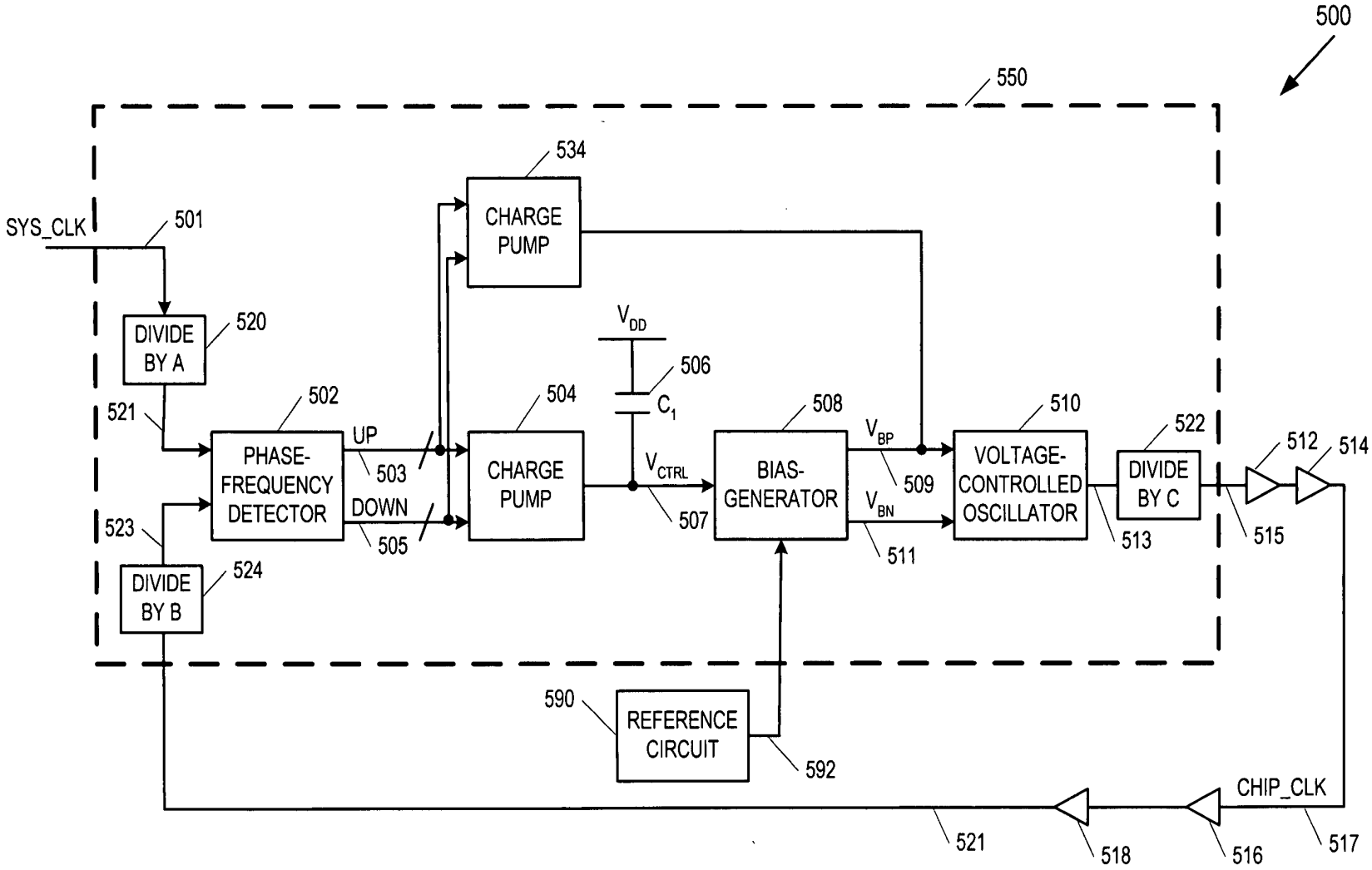
500
550
534
CHARGE PUMP
SYS_CLK
501
DIVIDE BY A
520
V_{DD}
506
C_1
521
502
PHASE-FREQUENCY DETECTOR
UP
503
DOWN
505
504
CHARGE PUMP
V_{CTRL}
507
508
BIAS-GENERATOR
V_{BP}
509
V_{BN}
511
510
VOLTAGE-CONTROLLED OSCILLATOR
522
DIVIDE BY C
513
512
514
515
523
DIVIDE BY B
524
590
REFERENCE CIRCUIT
592
CHIP_CLK
521
518
516
517

Figure 3

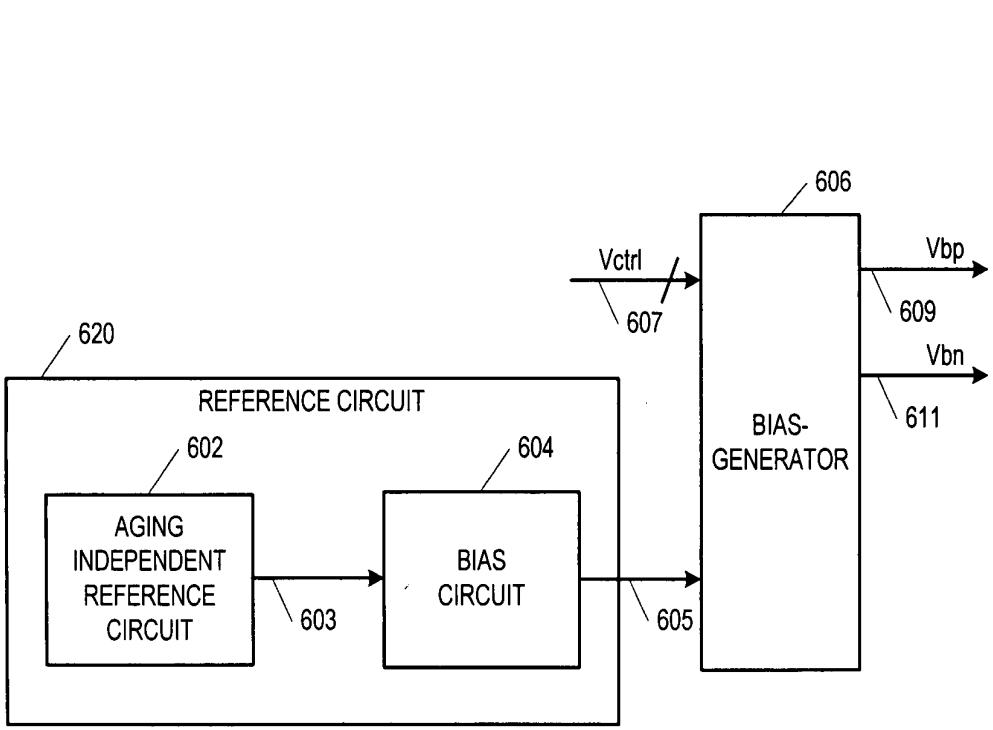
600
606
Vctrl
607
Vbp
609
Vbn
611
620
REFERENCE CIRCUIT
602
AGING INDEPENDENT REFERENCE CIRCUIT
603
604
BIAS CIRCUIT
605
BIAS-GENERATOR

Figure 4

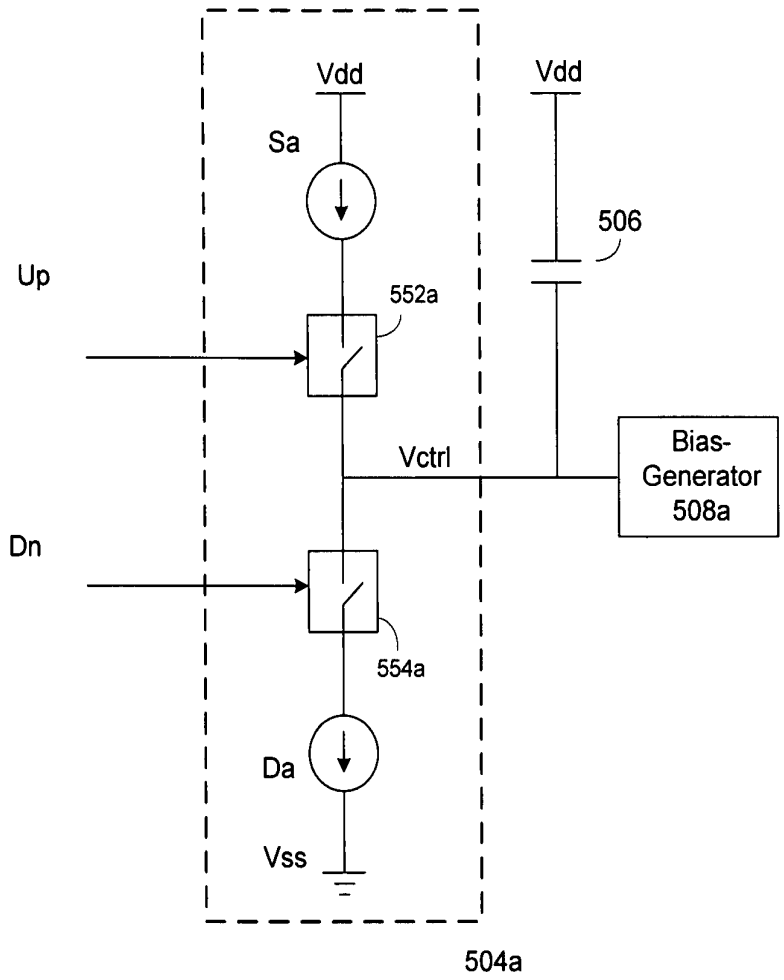

Figure 5a

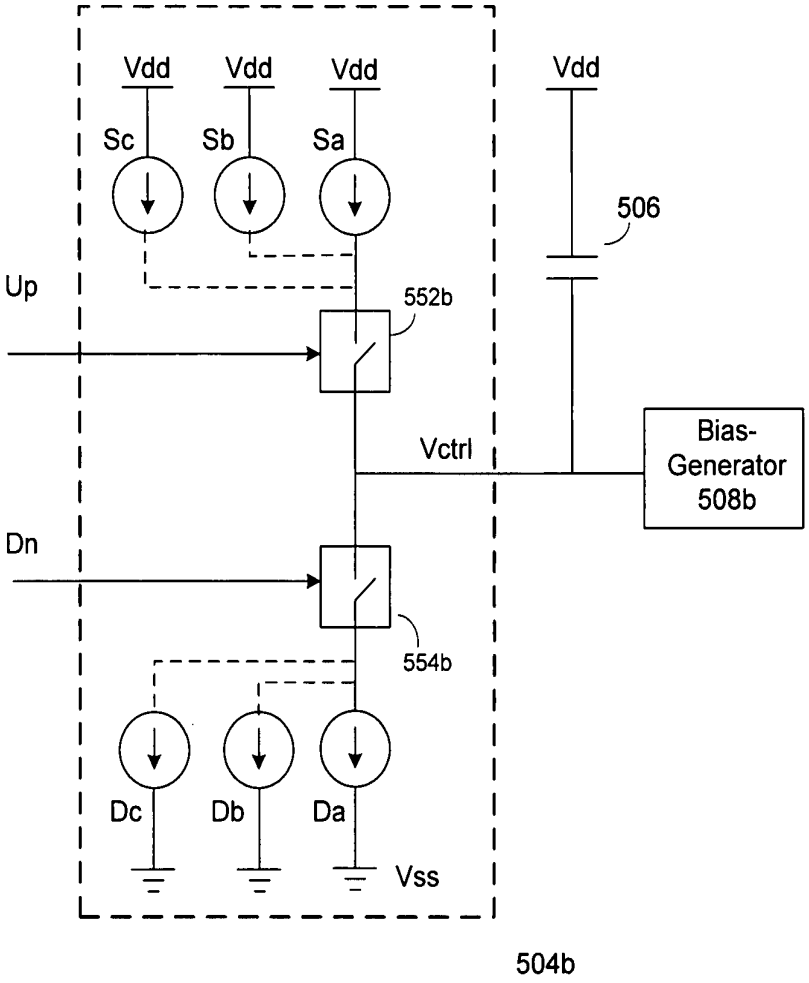

Figure 5b

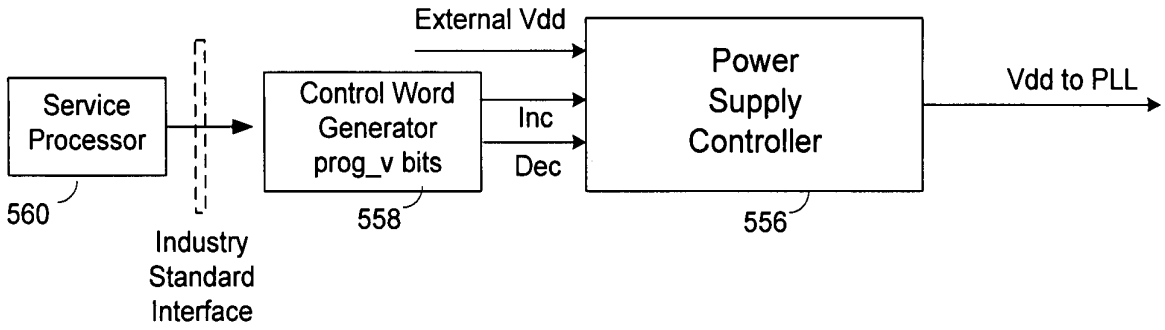
External Vdd
Service Processor
Control Word Generator prog_v bits
Inc
Dec
Power Supply Controller
Vdd to PLL
560
Industry Standard Interface
558
556

Figure 6

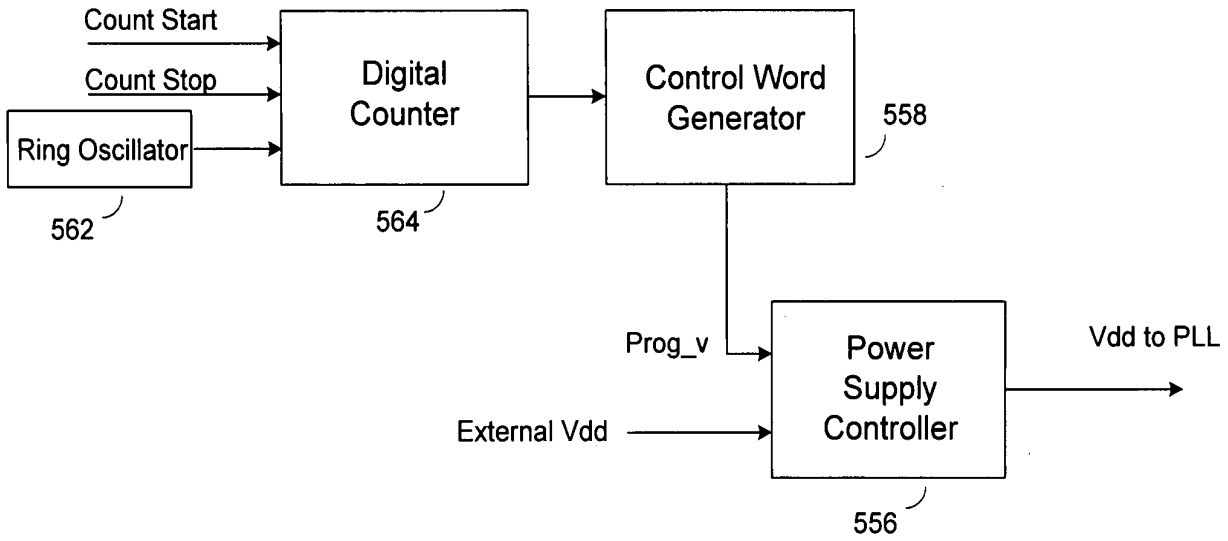
Count Start
Count Stop
Ring Oscillator
562
Digital Counter
564
Control Word Generator
558
Prog_v
External Vdd
Power Supply Controller
556
Vdd to PLL

Figure 7

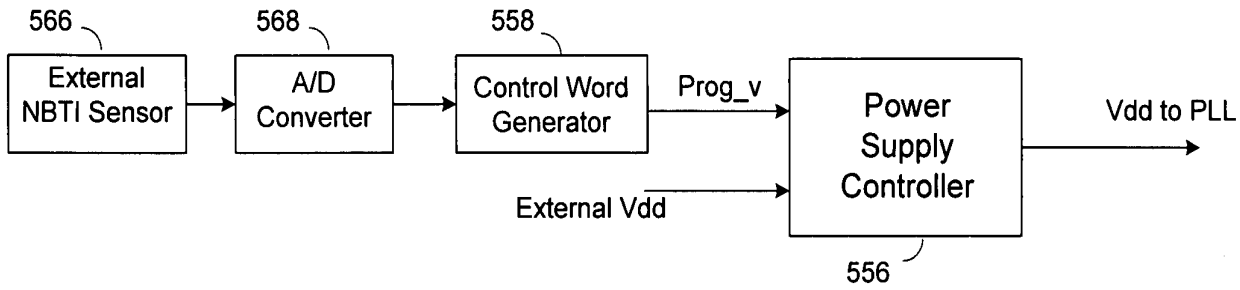
566
External NBTI Sensor
568
A/D Converter
558
Control Word Generator
Prog_v
Power Supply Controller
Vdd to PLL
External Vdd
556

Figure 8

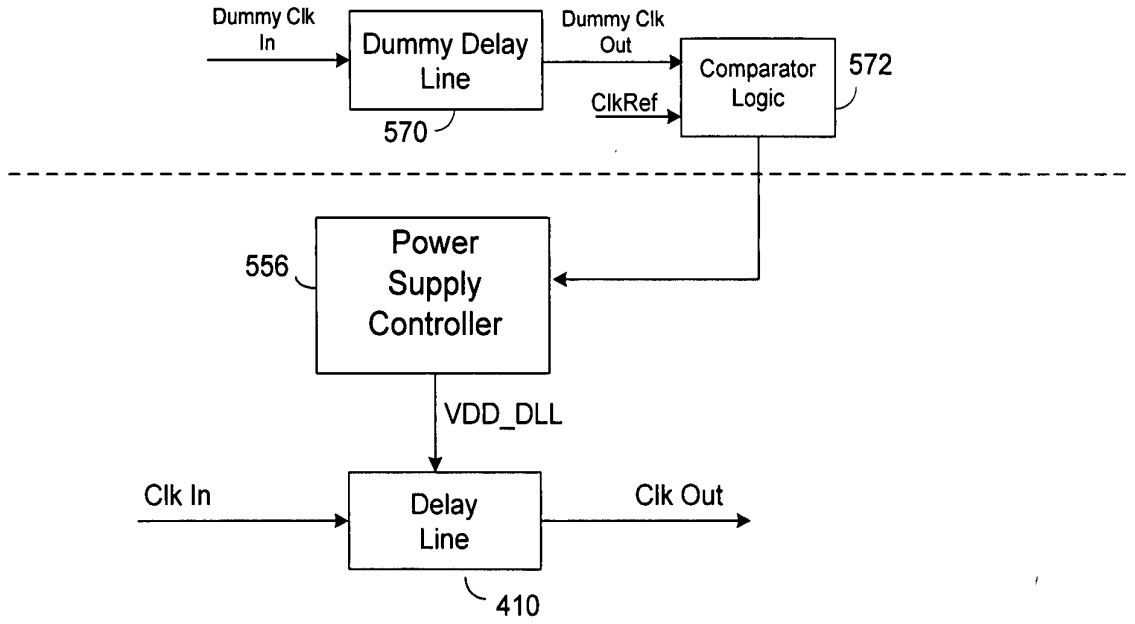
Dummy Clk In
Dummy Delay Line
570
Dummy Clk Out
ClkRef
Comparator Logic
572
556
Power Supply Controller
VDD_DLL
Clk In
Delay Line
410
Clk Out

Figure 9

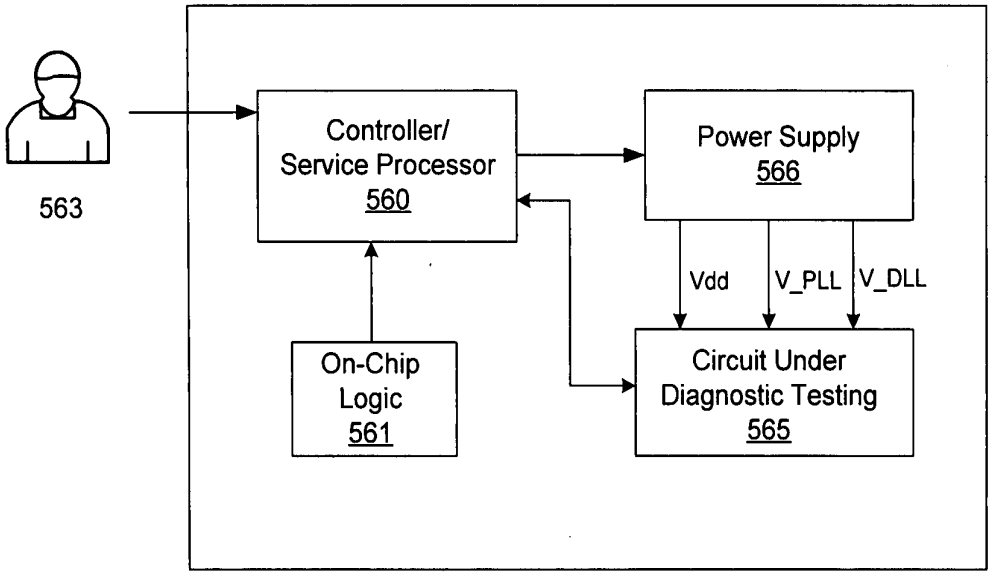
563
Controller/
Service Processor
560
Power Supply
566
Vdd
V_PLL
V_DLL
On-Chip
Logic
561
Circuit Under
Diagnostic Testing
565

Figure 10

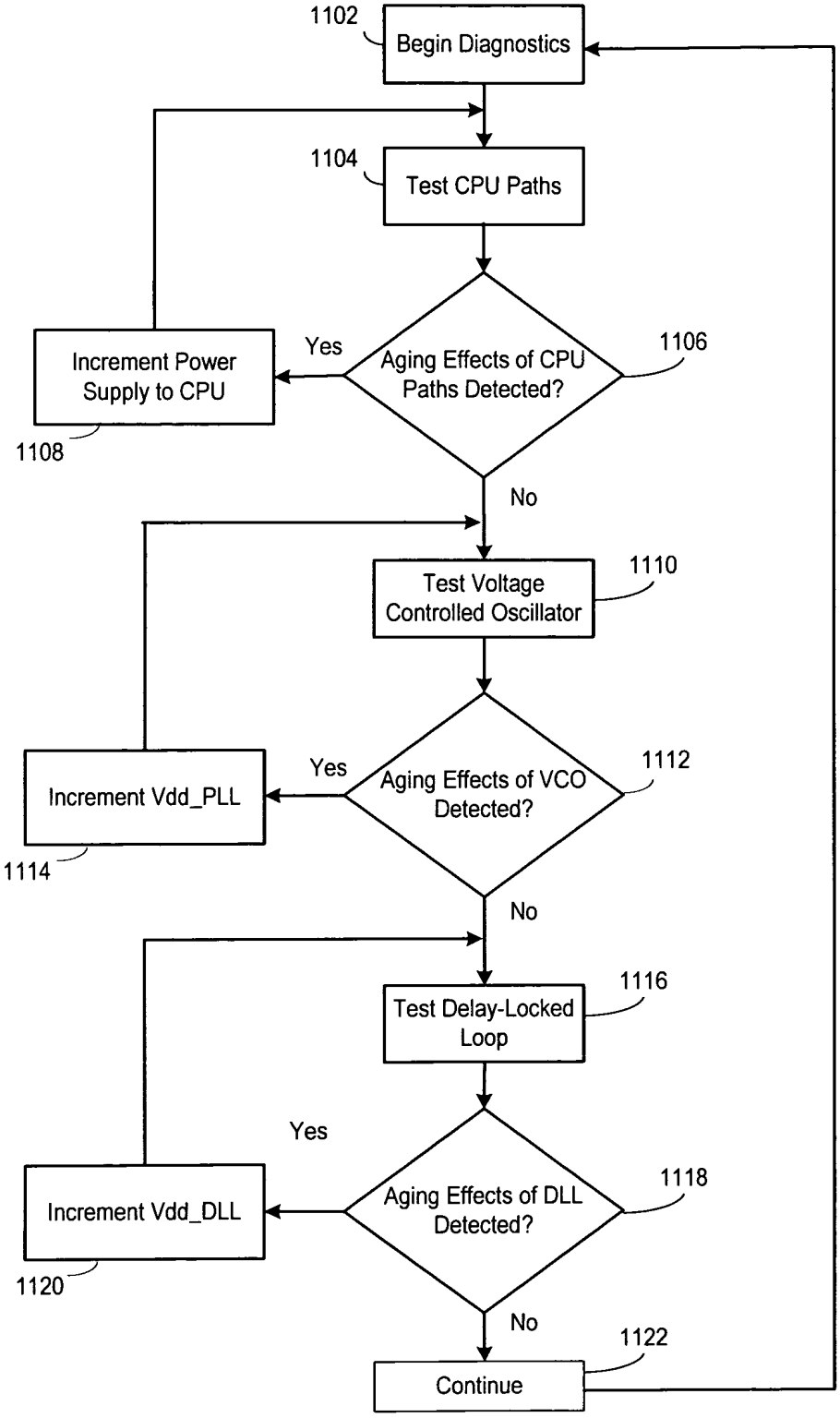
1102
Begin Diagnostics
1104
Test CPU Paths
Aging Effects of CPU Paths Detected?
1106
Yes
Increment Power Supply to CPU
1108
No
Test Voltage Controlled Oscillator
1110
Aging Effects of VCO Detected?
1112
Yes
Increment Vdd_PLL
1114
No
Test Delay-Locked Loop
1116
Aging Effects of DLL Detected?
1118
Yes
Increment Vdd_DLL
1120
No
Continue
1122

Figure 11